SUB D1 C1

17. (Twice Amended) A method for forming a contact hole, comprising:

depositing a dielectric layer upon first and second laterally spaced gate structures on a semiconductor layer comprising isolation regions, wherein the dielectric layer comprises doped silicon oxide having a phosphorus concentration of less than approximately 6 wt. %;

etching a first portion of the dielectric layer with a first etch chemistry, wherein the first etch chemistry is substantially free of hydrogen; and

etching a second portion of the dielectric layer with a second etch chemistry, wherein a thickness of the second portion of the dielectric layer is greater than approximately one half of a height of the first and second gate structures.

SUB D1 C2

21. (Amended) A method for forming a self aligned contact hole, comprising:

etching a first portion of a substantially continuous dielectric layer adjacent to a gate structure with a first etch chemistry substantially free of hydrogen sufficiently to expose a sidewall spacer of said gate structure, wherein the dielectric layer comprises doped silicon oxide having a boron concentration of less than approximately 5 wt. %; and

etching a second portion of the substantially continuous dielectric layer with a second etch chemistry comprising a hydrofluorocarbon etchant sufficiently to expose a substrate under said substantially continuous dielectric layer.

REMARKS

Claim 19 has been canceled. Claims 17 and 21 have been amended. Claims 1-5, 7-18, and 20-27 are currently pending in the captioned case. Further examination and reconsideration of the presently claimed application are respectfully requested.